Zelinda Ireland Ltd

Zelinda Company Background

- Incorporated in 2000
- Fully Focused on Space communications
- Based in Waterford, in the South East of the Republic of Ireland
- Ownership
  - 67% with the founding directors
  - 33% with Celestia STS (the Netherlands)

Zelinda Capability & Competitiveness

- Fully Focused on Space Communications:
  - Specialised
    - only DSP (inc ADC & DAC) & architecture around DSP
  - DSP Designs are predictable (spuriae, noise) “all design – no development”
  - Innovative algorithms & Architectures
    - Using sampling schemes that move aliases out of band
    - One bit sampling and dither (simple, provides automatic ALC)
  - Innovative Implementations
    - Deep understanding of algorithms allows simplification of implementation
    - Combining successive DSP blocks into single entity (eg Interpolator & Upconvertor)
    - Several functions provided by single Module (eg FFT does DCAAS Dynamic Channel Activity Assignment System & Rx Channelisation)
    - Scaling to minimise quantisation noise & hence number of bits (eg in sinewave LUTs)
    - Hardware and Software implementations

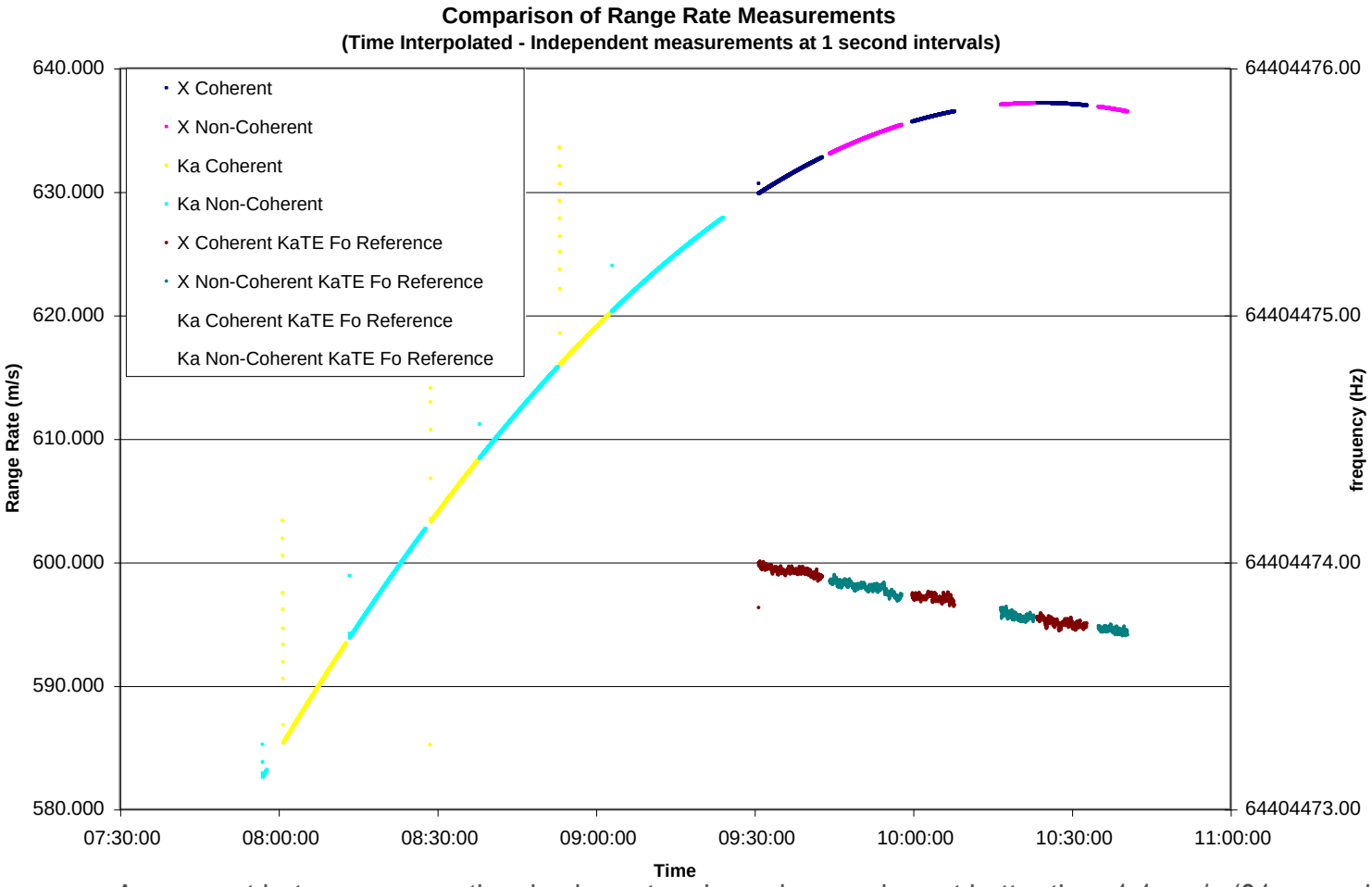
Project & Custom Base

Project	Prime Contractor	Customer
IFM	MDA	JAXA
KaTE Transponder	Astrium Ottobrunn	ESTEC
BEM modem	Callisto	EuMetSat
TTC Transponder	Honeywell	ESA / Fomosat / LuxSpace
NRX	Zelinda	ESTEC
NMDU	SSBV	Galileo
Ka-Antenna Upgrade	Callisto	ESOC
TTCF Modem	SSBV	Galileo
Galileo DST Transponder	Tesat (Backnung, DE)	Galileo
C-Band Transmitted DU	Honeywell	Exact Earth
EDTE Modem	SSBV	Airbus
Protocol	Arpsoft	ESOC
EcomTec Study	Callisto	ESTEC
AR4JA LDPC Codec	BAE Systems	ESOC
FAT Transponder	Honeywell	ESTEC
ABBM Modem	Celestia STS	ESTEC
VHDR	Tesat (Backnung, DE)	ESTEC

Novel Range Rate Experiment (NRX)

- Contracted to ESA ESTEC
- Objective to prove the reliability and accuracy of a Zelinda Proprietary Non-Coherent two way range rate measurement technique.
- Design & Development of a ground demodulator to measure groundstation integrated Rx & TX carrier phase which together with spacecraft Integrated Rx & TX carrier phase yields range rate & spacecraft Tx frequency.
- KaTE Ka band Tx Power only 20 mW hence ground demodulator designed to track down to C/No 16 dBHz.
- Experiment conducted during Lunar insertion

KaTE Range Rate Results



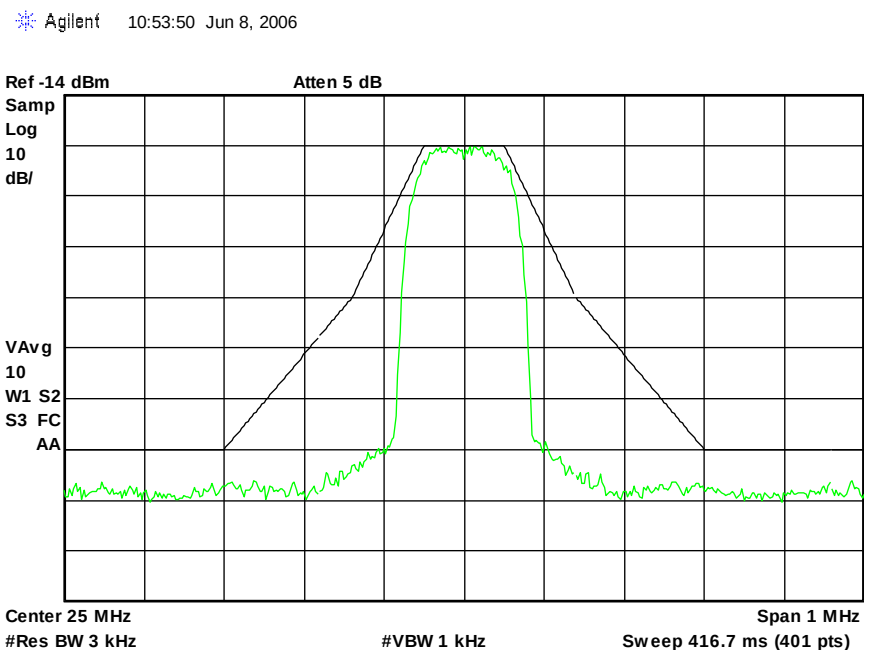
- Agreement between conventional coherent and novel non-coherent better than 1.1 μm/s (31 second average)
- Measurement noise less than 0.160 mm/s (31 second average)

S & X Band Transponder

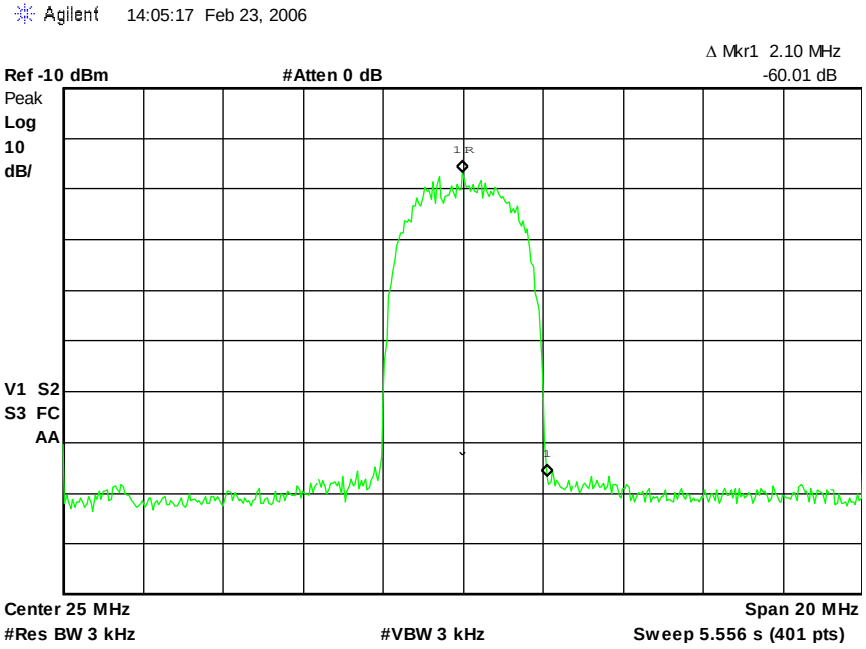
- Developed Jointly with Honeywell (UK)
- Flexible Rx Modulation schemes and data rates
    - PCM/BPSK/PM, SP-L/PM, SP-L, or BPSK upto 1 Mbps
  - Flexible Tx Modulation schemes and data rates
    - BPSK, SPL, SRRC OQPSK (32k – 6.25 Mbps)
  - Flexible RF frequencies & Tx Power
    - RX/TX channel frequency user selectable (synthesized LOs controlled by Privileged Commands)

- Joint architectural design with Honeywell
- Zelinda designed FPGA
  - Innovative one-bit IF sub-sampling receiver concept
    - Thermal noise (or added dither) used to linearise
    - 5 times over sampled WRT signal bandwidth
    - IF around "n -1/5" of sampling rate (not ¼)
    - Sampling at high IF of 190 MHz where SAW Rx filter small & lower loss
    - Single stage Rx downconversion
    - FPGA based (Actel RTAX)
  - Coherent Turnaround and Tx SRRC filtering in Digital domain
  - Digital upconversion to first Tx IF

S & X Band Transponder Tx



200 kbps SRRC OQPSK



5 Mbps SRRC OQPSK

> 25 delivered :

Formosat, Esail, M3M, Cheops, Innosat….

DST – Dual Standard Galileo TTC Transponder

Initially aimed at Galileo FOC Satellites:

- DSSS – 2 kbps Rx & 50 kbps Tx using TDRSS 1023/261,888 long codes
- Rx - PCM/BPSK/PM using 16 kHz Subcarrier, Tx using BPSK/PM using 252 kHz subcarrier
- Transparent ranging channel supporting ESA standard code/tone ranging with TC echo suppression
- Exact Coherency (with configurable turnaround ratio)

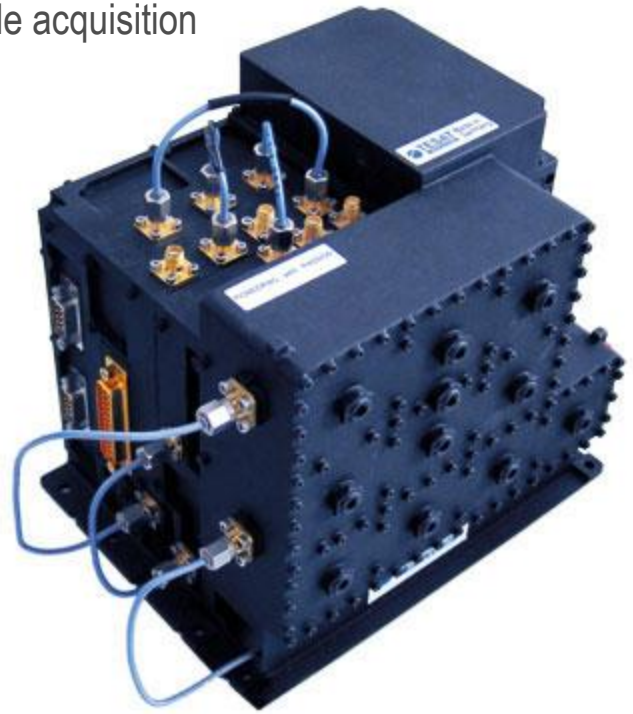
Developed to include

- X-Band or S-Band versions
- FM receive
- BPSK receive
- SPL/PM receive
- SPL Tx
- BPSK Tx upto 6 Mbps
- SRRC OQPSK Tx upto 12 Mbps

DST – Dual Standard Galileo TTC Transponder

Zelinda designed FPGA in VHDL.

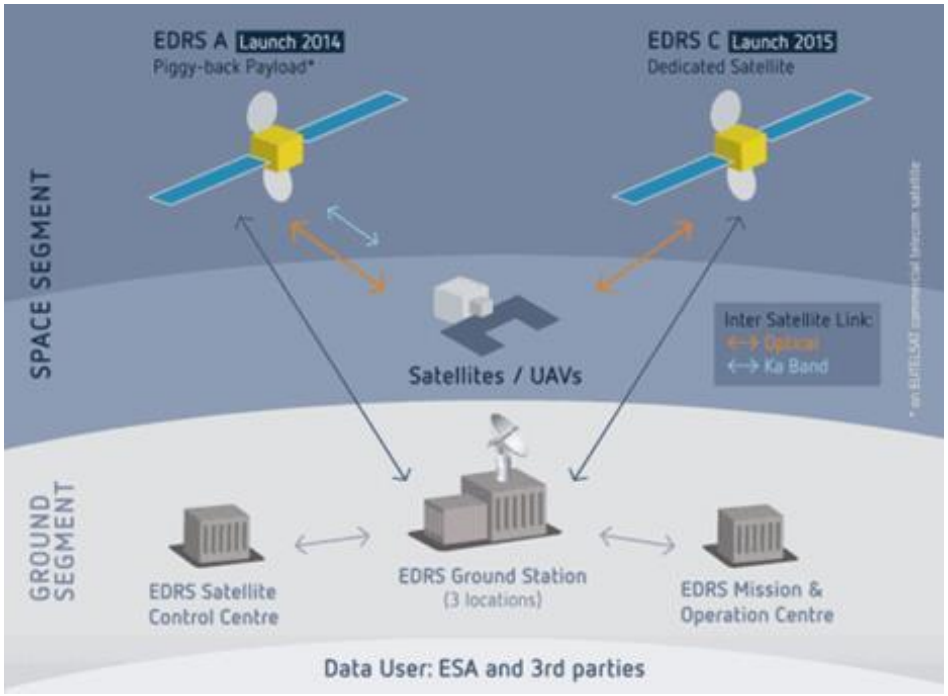
- 70 MHz Rx IF sampled at 40 Msps
- 140 MHz Tx IF sampled at 200 Msps
- Parallel correlator implemented in time domain for DSSS code acquisition
- Control and monitoring via serial interface
- Implemented in Microsemi RTAX FPGA without multipliers



44 units now flying

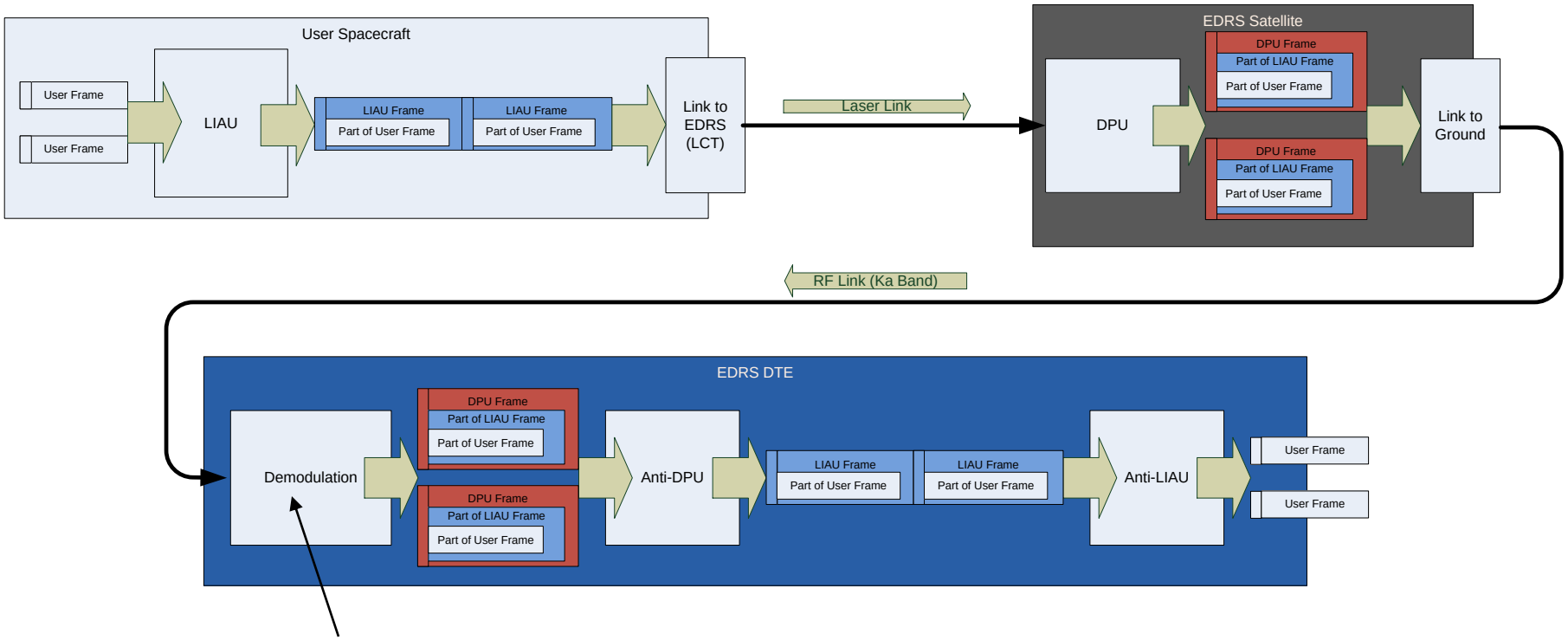
EDTE Demodulator for European Data Relay System

- EDRS is multiple GEO satellites providing data relay from LEO satellites to Earth.



EDTE Demodulator for European Data Relay System

Overall Data Flow

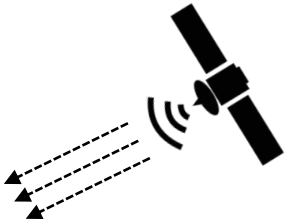


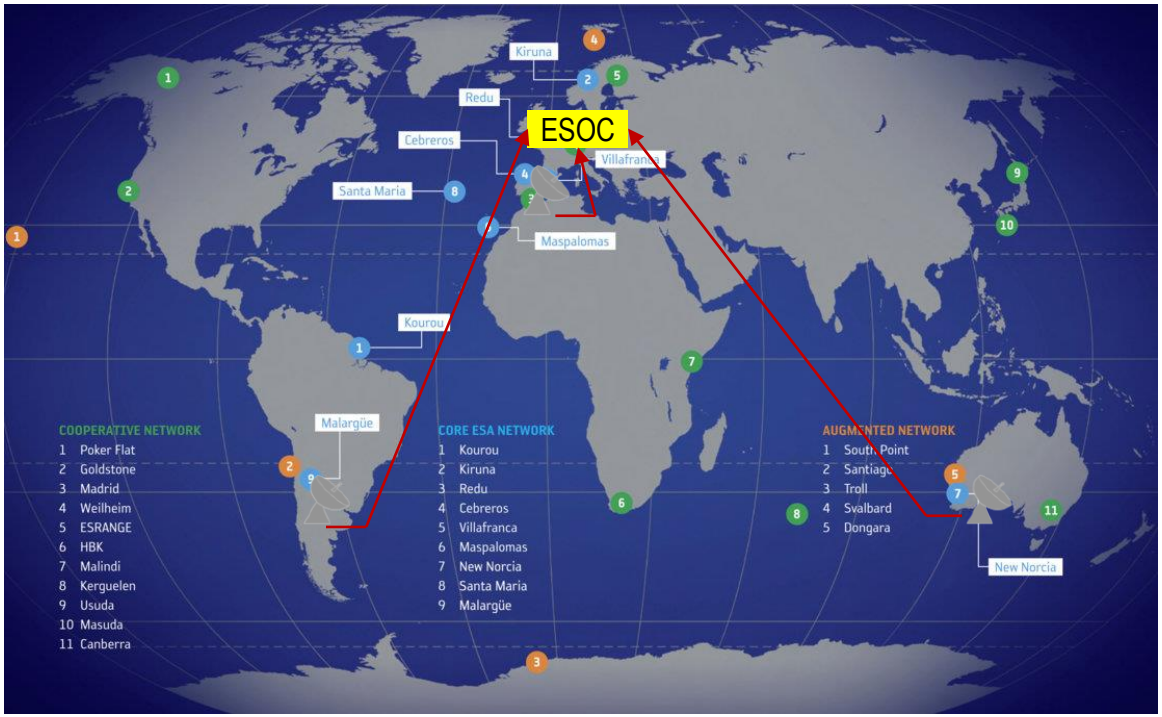
Zelinda Designed & implemented 2.4 Gbps (4 channels x 600 Mbps) OQPSK FPGA Demodulator using 1.2 Gsps processing 8 samples in parallel.

Operated down to Es/No < -1.0 dB with implementation loss < 0.25 dB

Protocol – Prototype Offline Correlator

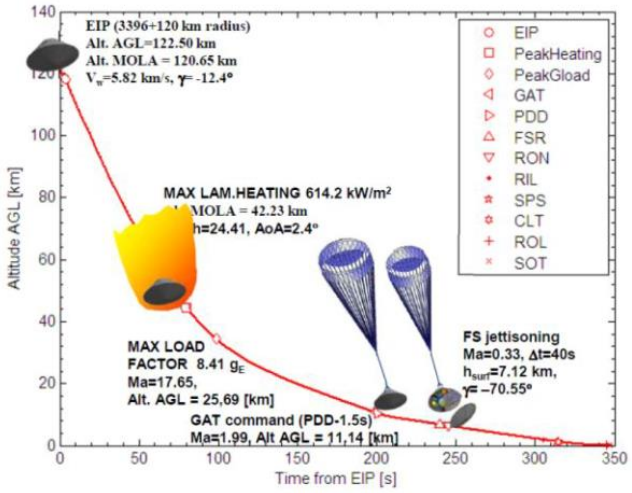
- Open-loop recorded signals from 2/3/4 Deep Space antennas are combined at ESOC to improve received SNR.
- Zelinda developed C++ program implementing “Sumple” Algorithm to acquire and track relative phases and delays of signals.
- Developed with Arpsoft (Italy).
- Successfully tested using Cebreros (Spain) and Malargüe (Argentina) with both
- Mars Express and ExoMars

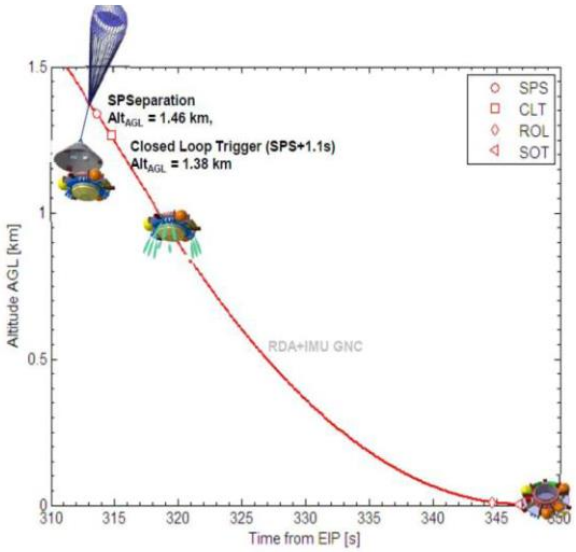


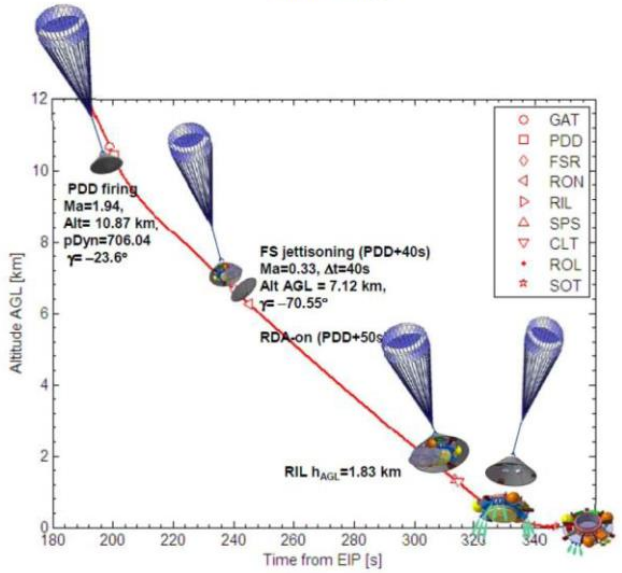


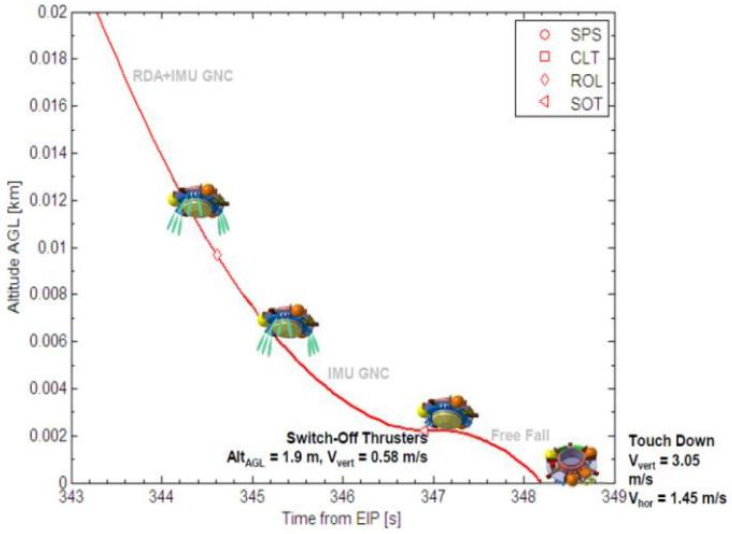
EComTec

Entry, Descent and Landing COMmunications TECnology Study









Example EDL phase from ExoMars 2016

EComTec

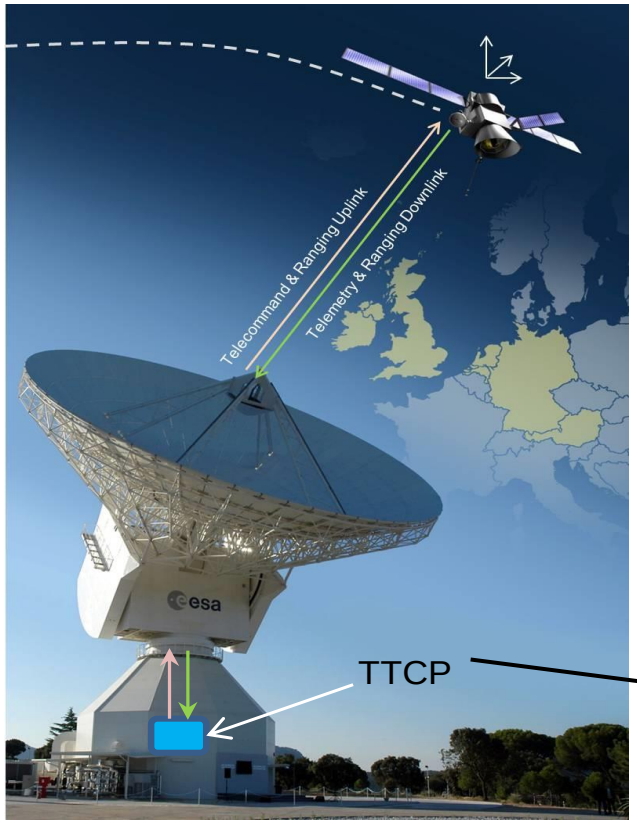
Entry, Descent and Landing COMmunications TECnology Study

- Intended for Direct to Earth communications at X-Band from Probe with very high Doppler dynamics during EDL and low gain omni antenna.

- Low data rate “Special MFSK” modulation scheme developed by JPL using Carrier phase modulated by square wave at tone frequency. Supports Low data rates - 1 to 8 bps.

- Zelinda developed a Joint detection scheme for carrier and sidebands offering a 7.3 dB performance improvement over JPL scheme. Supported 2 bps at C/No = 16.5 dBHz

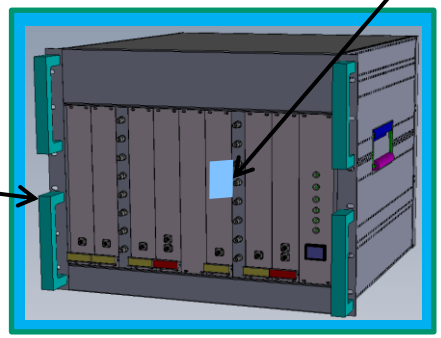
AR4JA LDPC Codec for ESOC's TTCP



LDPC provides > 1 dB better than Concatenated Conv/RS

Developed as a self contained and independent "plug-in"

Altera Stratix V



LDPC Codec

Used Sum Products Algorithm with Min*() combining at Check Nodes.

Bit true and delay true C++ model developed and validated first.

C++ model adapted to include automatic writing > 6000 lines of VHDL code.

AR4JA LDPC Decoder

CCSDS standard developed by JPL provides 9 combinations:

- 3 information block sizes 1024, 4096 and 16364 bits
- 3 code rates. ½, 2/3, 4/5.

Aimed at Deep space, but higher code rates than Turbo.

Performance using 350 MHz clock in Altera Stratix V:

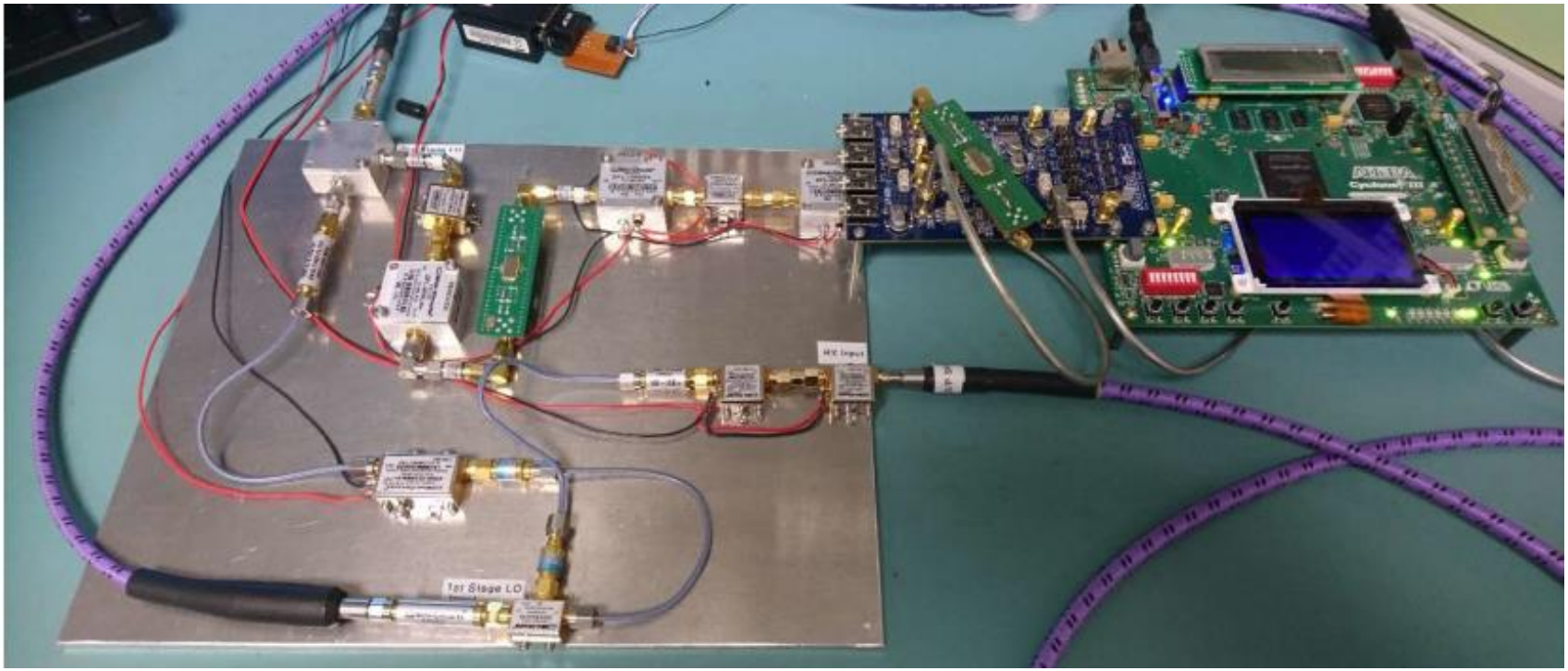
- BER Within ~0.02 dB of reference curves for < 200 iterations
- 25 Mbps for k = 1024 with 50 iterations
- 13 Mbps for k = 4096 with 100 iterations
- 6 Mbps for all block sizes with 200 iterations
- Multiple decoders with elastic buffering used to provide > 75 Mbps

FAT Transponder

Flexible Autonomous Transponder Bread board

- X & Ka Band
- Autonomous Acquisition without ground station sweep using FFT
- Autonomous reacquisition of data modulated signal
- DSSS acquisition using frequency domain parallel correlator
- Autonomous Rx Modulation scheme detection:
  - DSSS
  - SPL/PM
  - PCM/BPSK/PM with subcarrier,
  - BPSK.
- Autonomous data rate detection using SSME algorithm
- In flight adjustable Rx and Tx channels and coherency ratio
- Regenerative PN Ranging, Transparent ranging, DSSS ranging
- One way range rate
- Flexible TM Downlink Modulation schemes (Subcarrier, SPL, BPSK, OQPSK, GMSK, DSSS)

FAT Transponder Breadboard

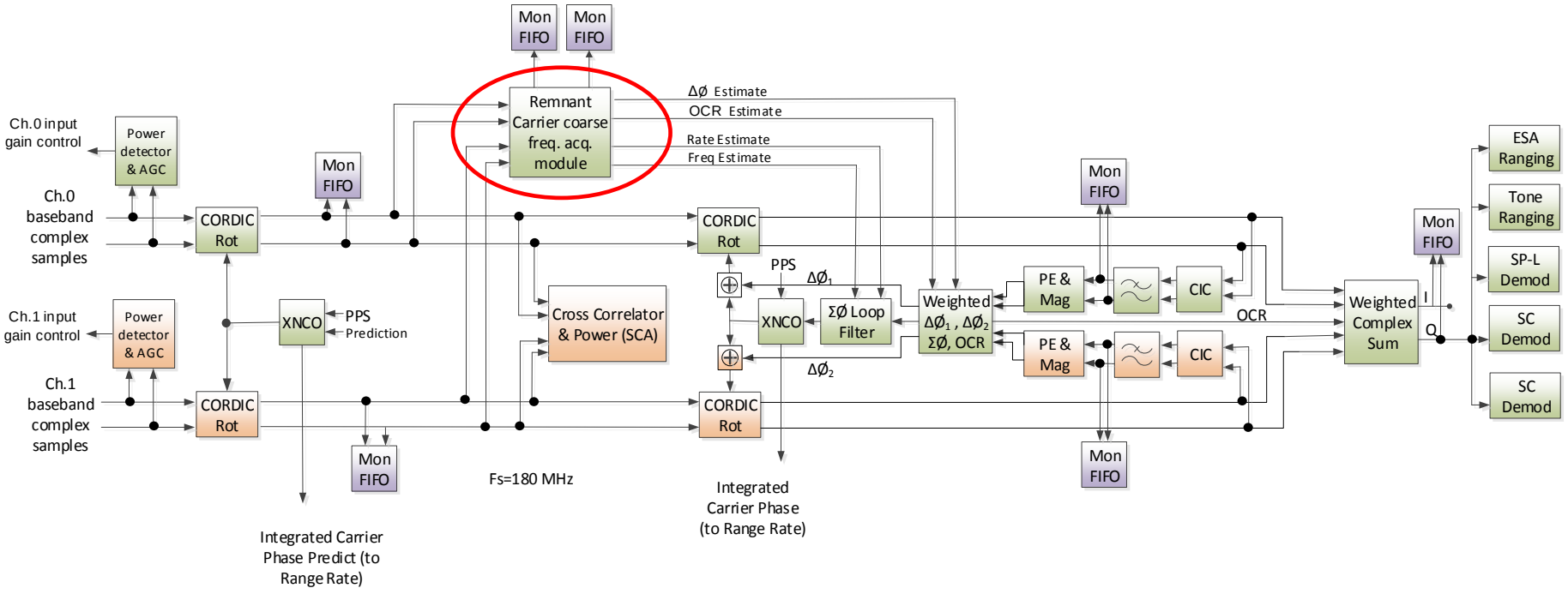


ABBM Modem

Advanced Base Band Modem

- Aimed at constellations and EGSE
- 4 channels including diversity combiner
- Fast Carrier & Diversity acquisition using FFT
- Supports 2 subcarriers per carrier
- Currently under development

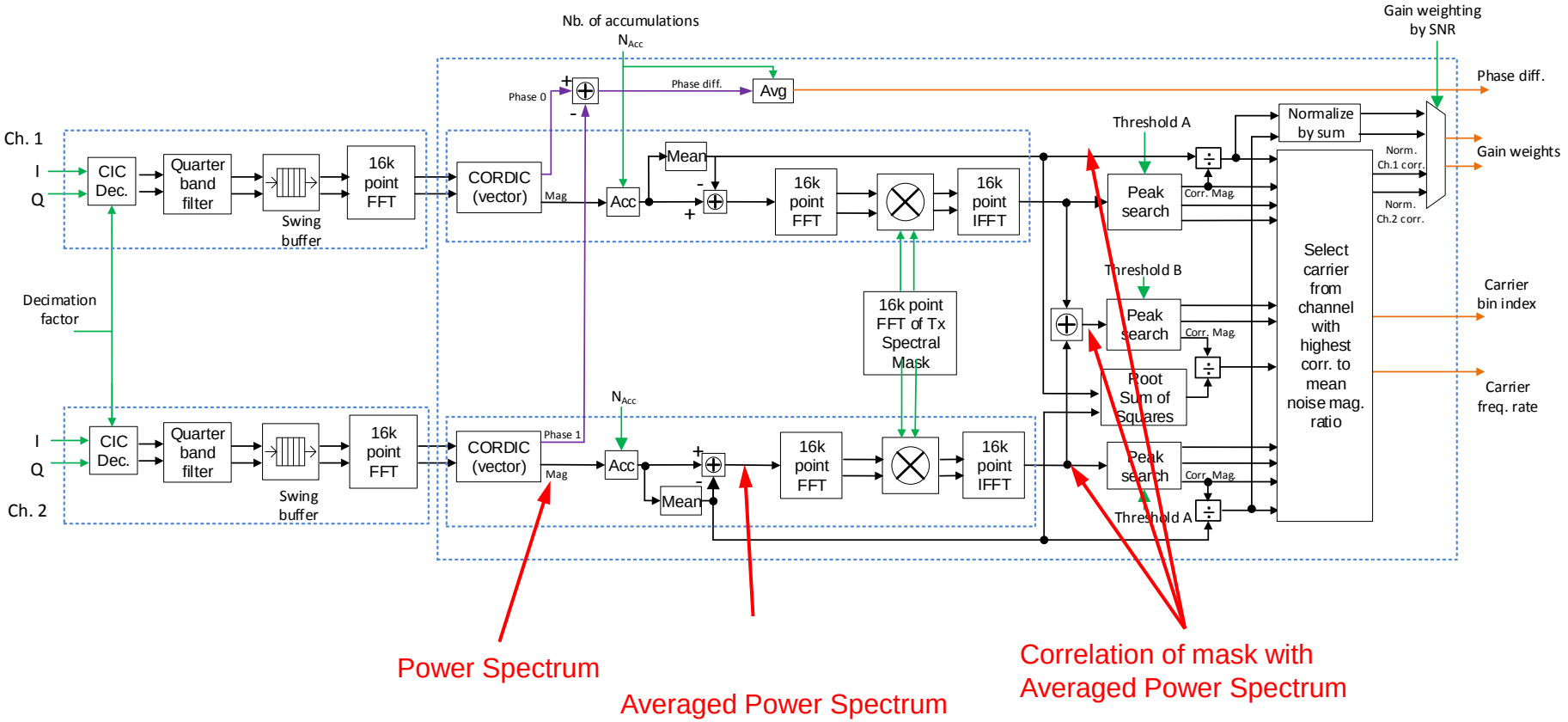
ABBM Modem - Overview



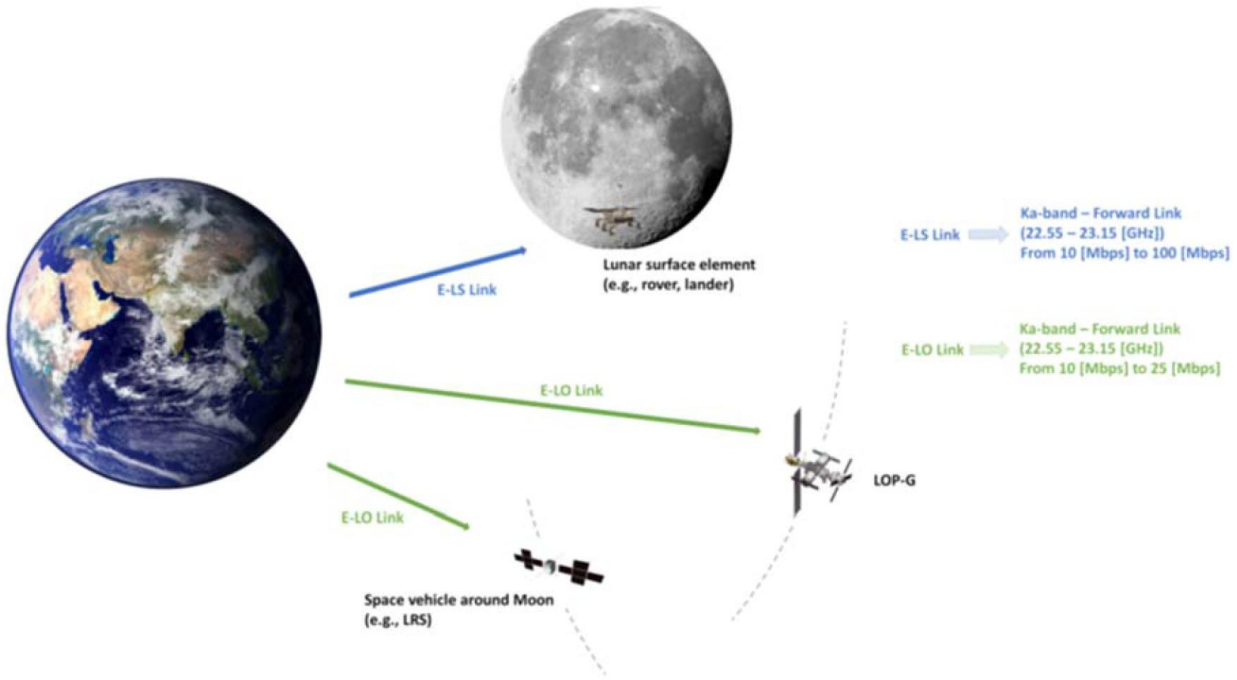
- 3 independent demodulators (above x 3)

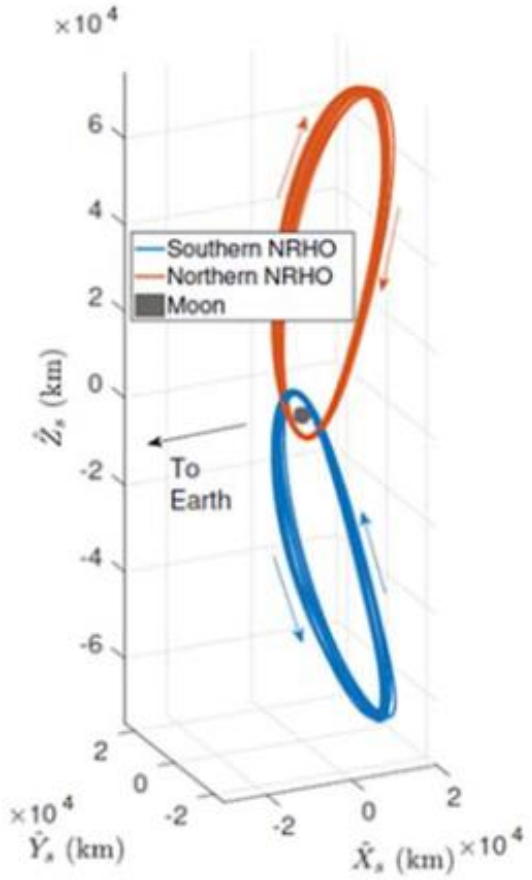
ABBM Modem - Initialisation

- Diversity Combination initialisation
- Carrier Frequency Acquisition



VHDR Very High Data Rate Receiver





Receiver for Lunar Relay Satellite in Near Rectilinear Halo Orbit (NRHO)

- Autonomous Symbol rate and Code rate detection
- SRRC OQPSK modulation scheme
- LDPC AR4JA codes (rates ½, 2/3 4/5, k = 16384)
- Symbol rates 10 – 100 Msps

Conclusion

- Zelinda have pre-existing tested VHDL modules to do many Transponder and Ground Modem functions.
- This VHDL is flexible and adaptable to different architectures (sampling rates, data rates, performance trade-offs)
- Zelinda is experienced in both DSSS and conventional Transponders and Ground Modems.
- Expertise includes Ranging (Tone/Code, RPN) and LDCP coding.
- Zelinda have designed several transponder digital units supporting multiple modulation schemes (SUT, Galileo, FAT).
- Zelinda offer a low risk route to successful project completion.